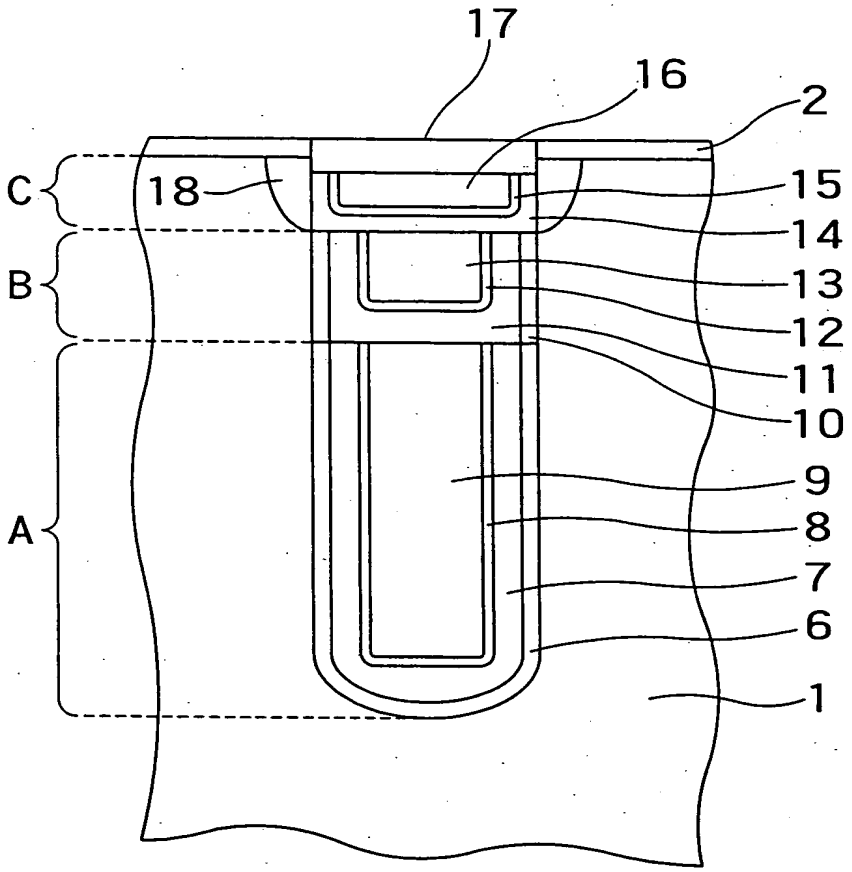


FIG. 1

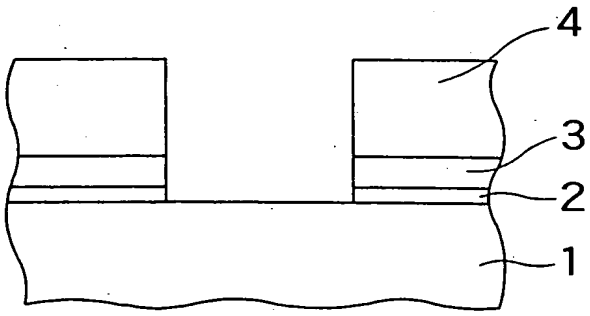


FIG. 2A

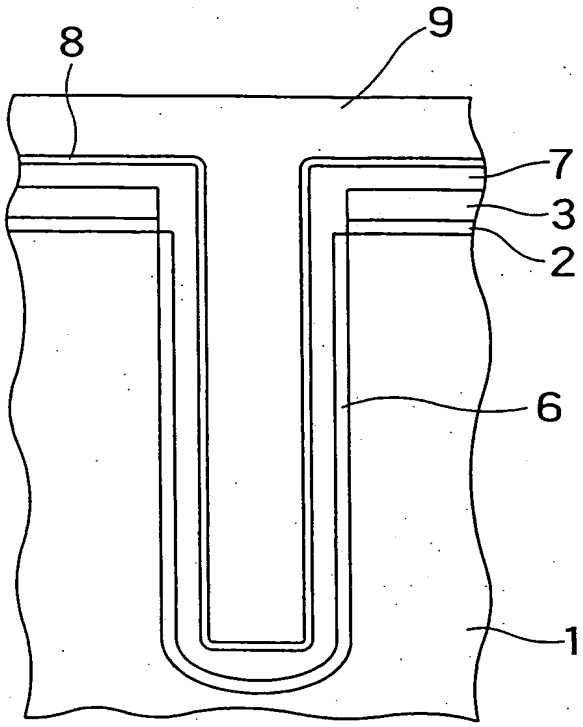


FIG. 2C

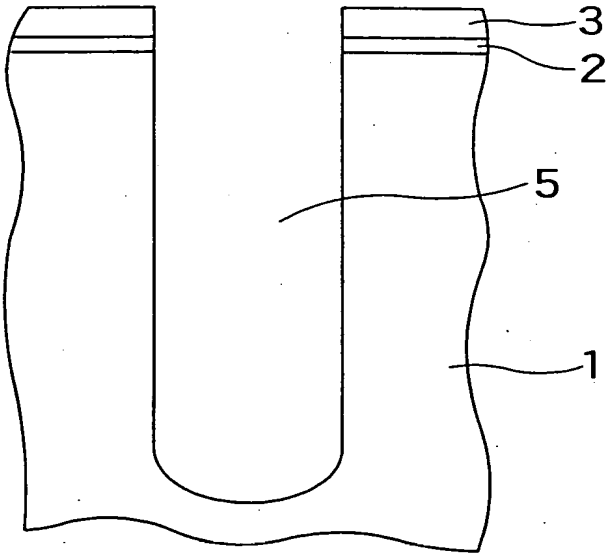


FIG. 2B

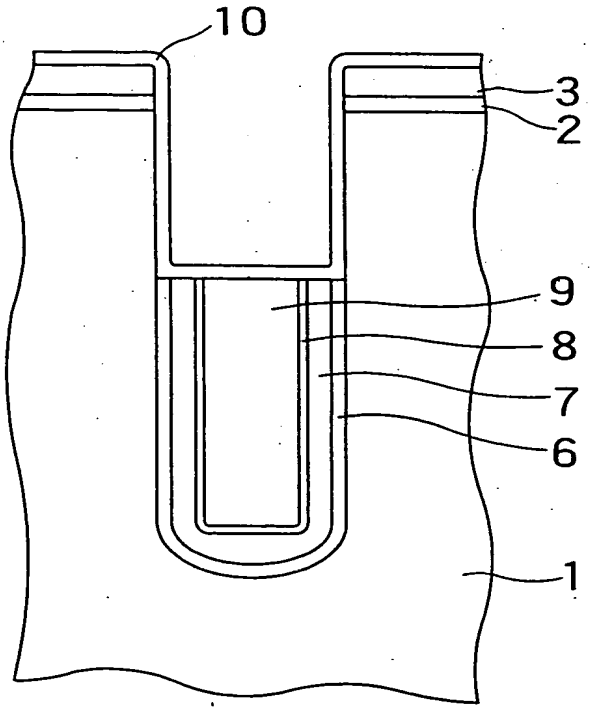


FIG. 2D

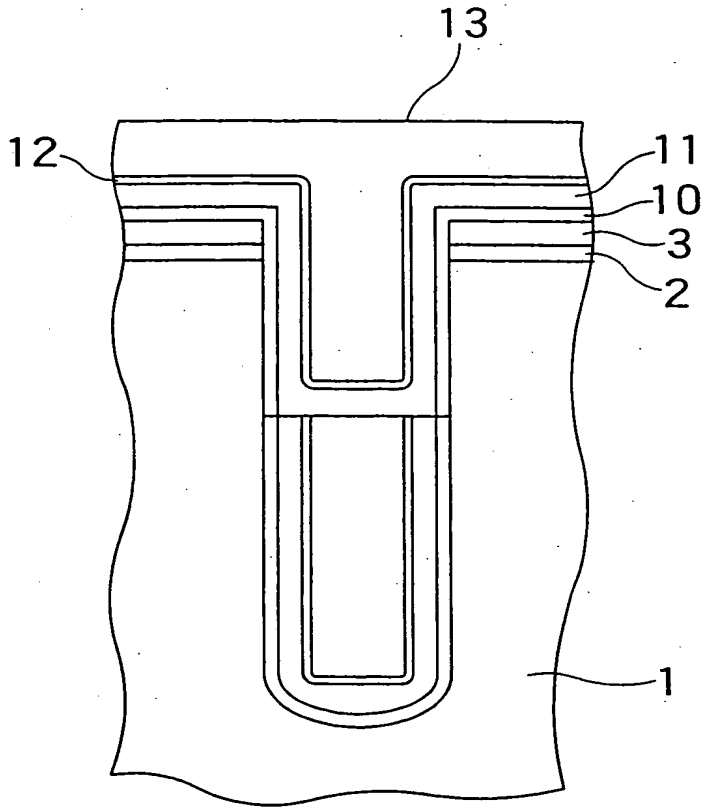


FIG. 3A

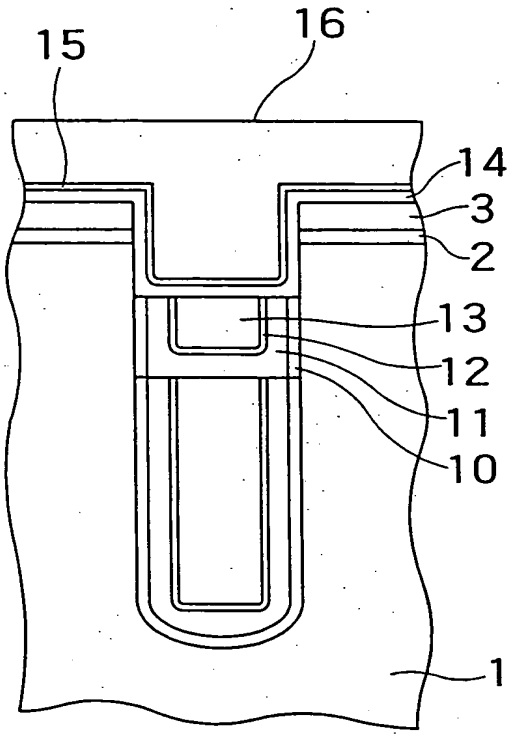


FIG. 3B

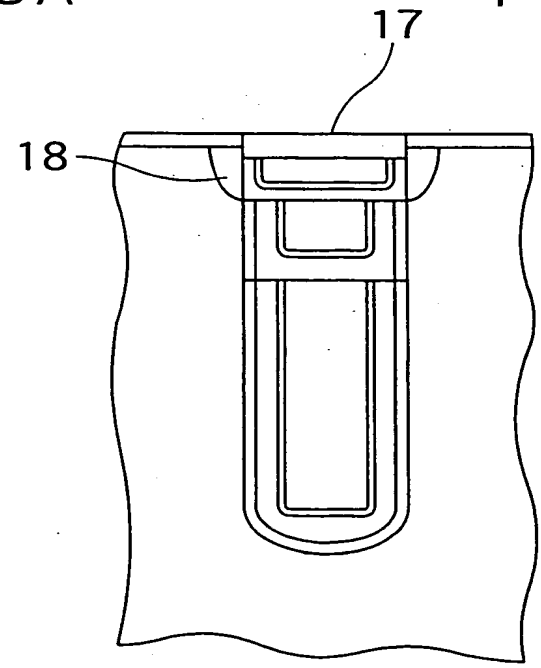


FIG. 3C

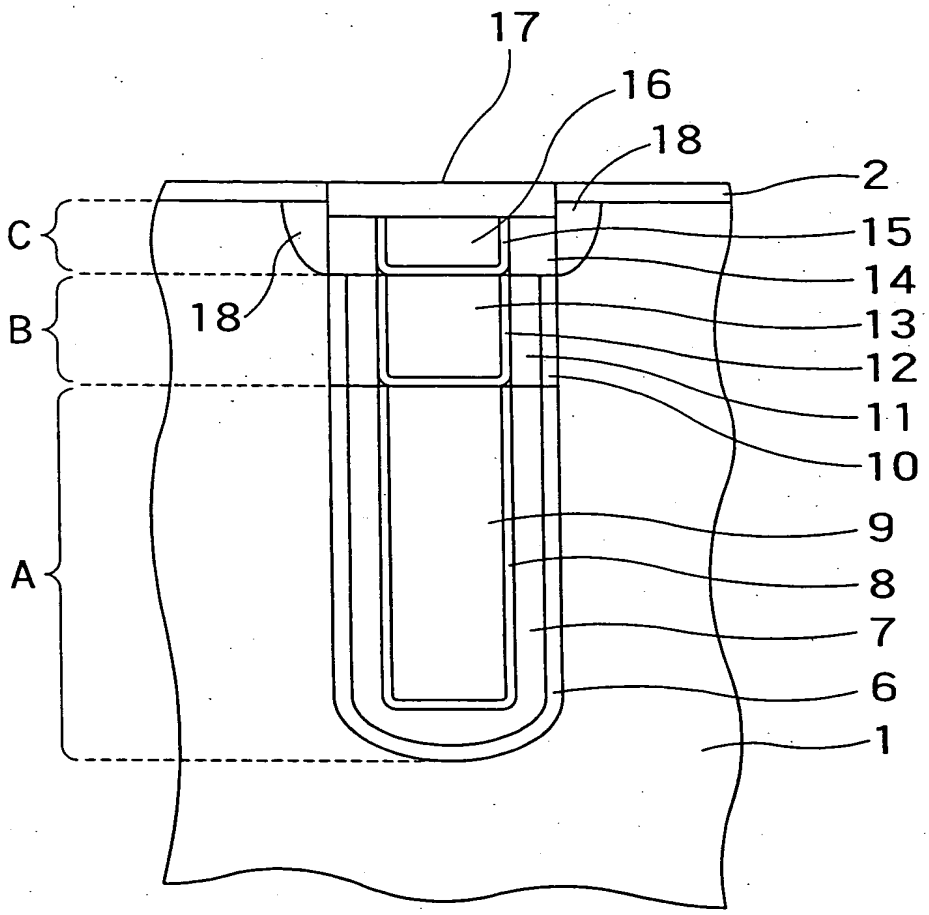


FIG. 4

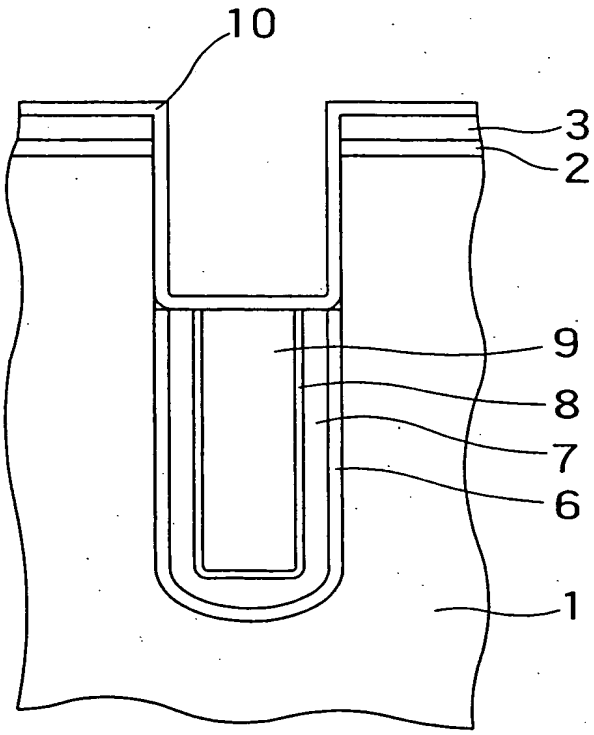


FIG. 5A

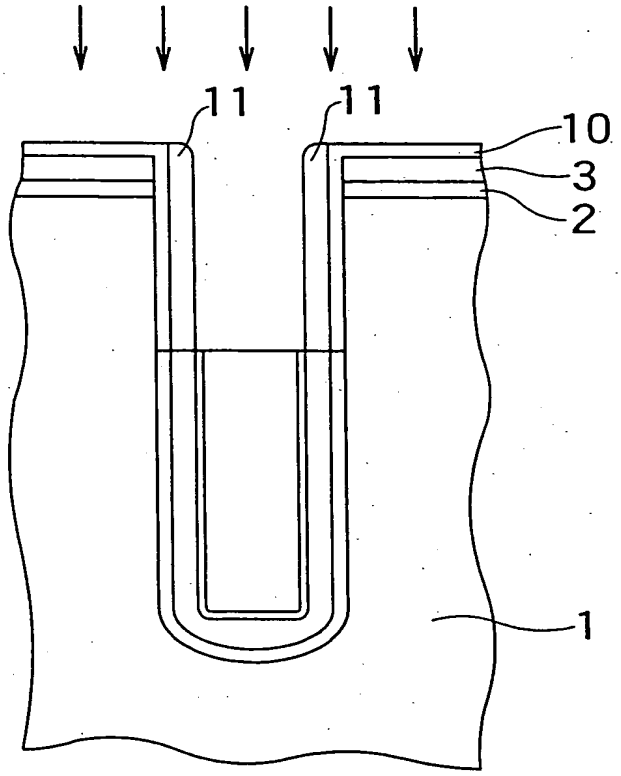


FIG. 5B

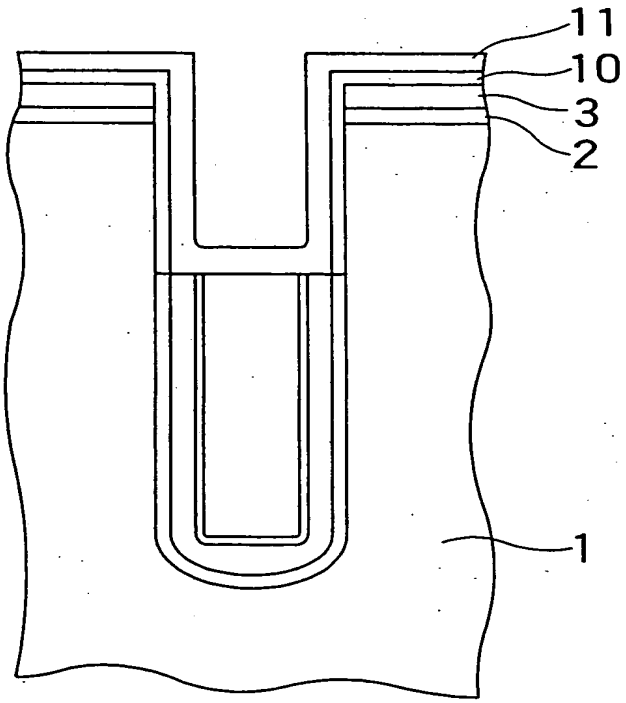


FIG. 5C

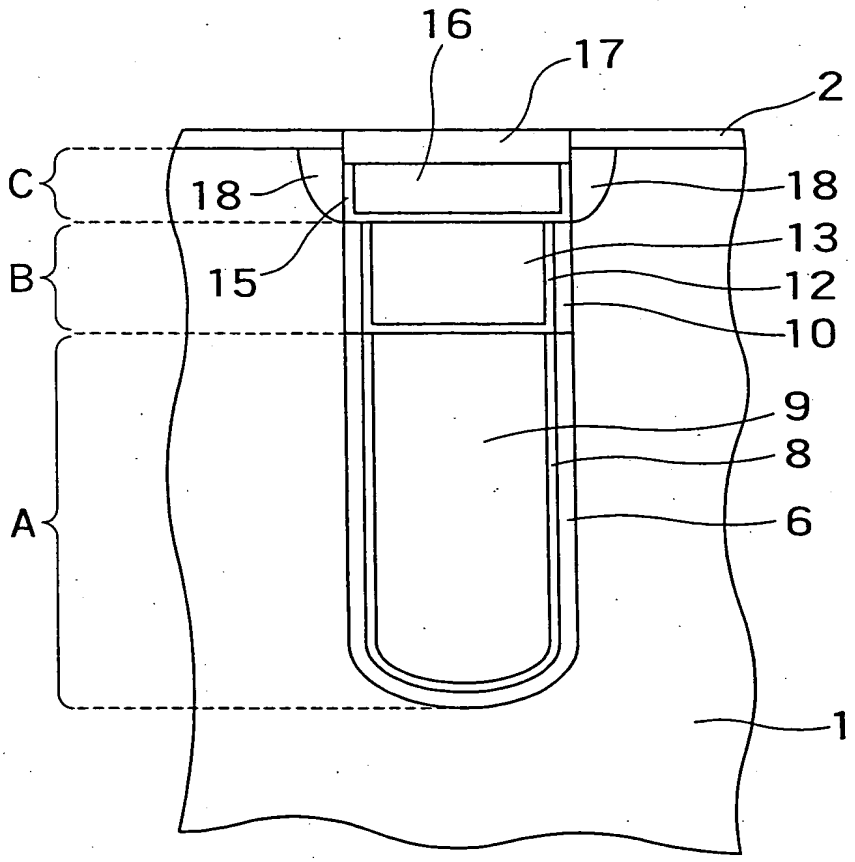


FIG. 6

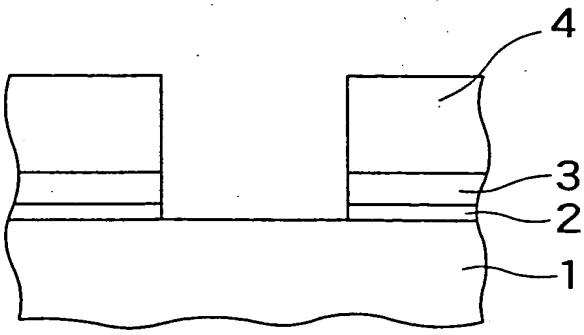


FIG. 7A

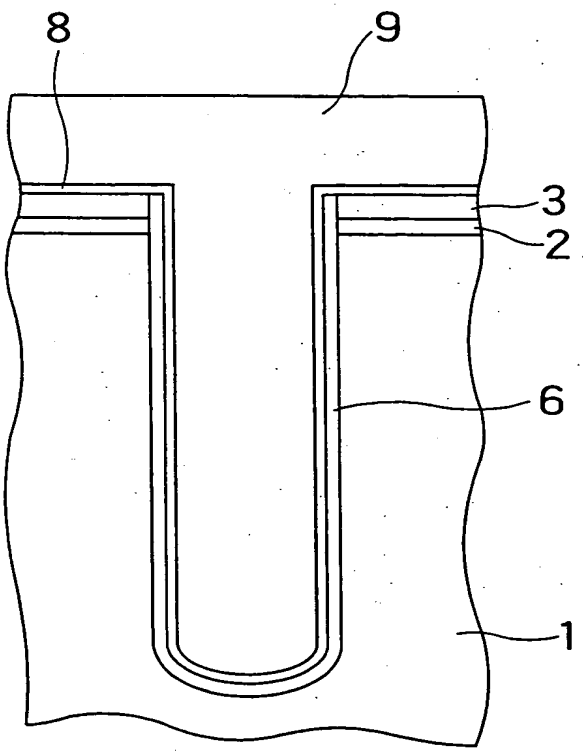


FIG. 7C

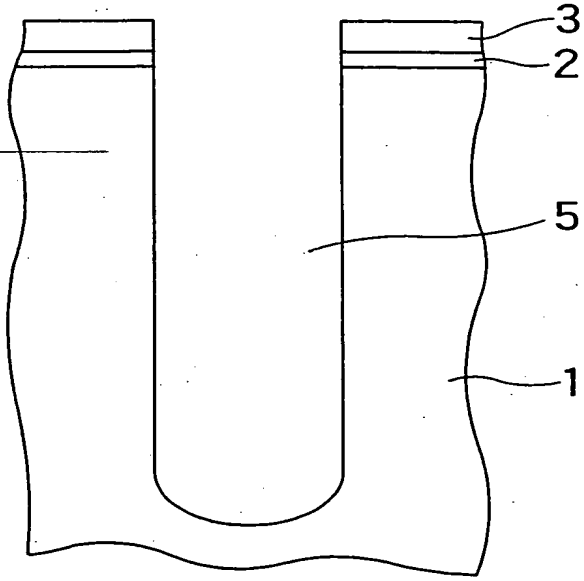


FIG. 7B

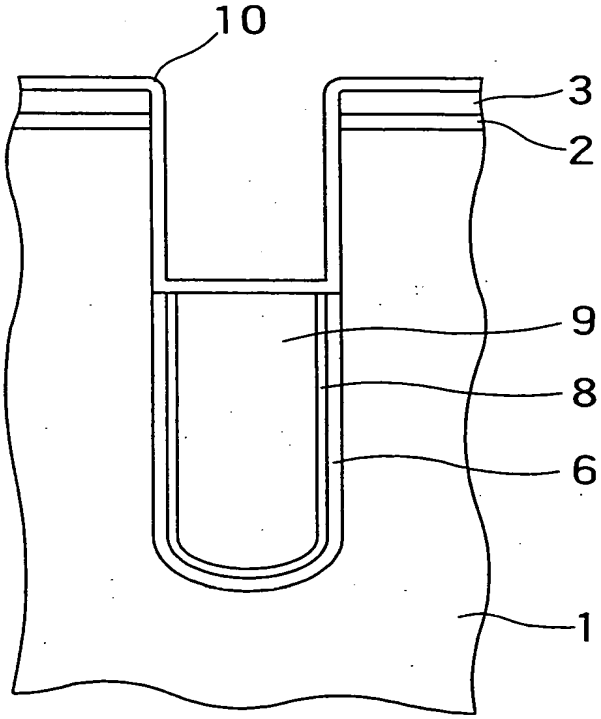


FIG. 7D

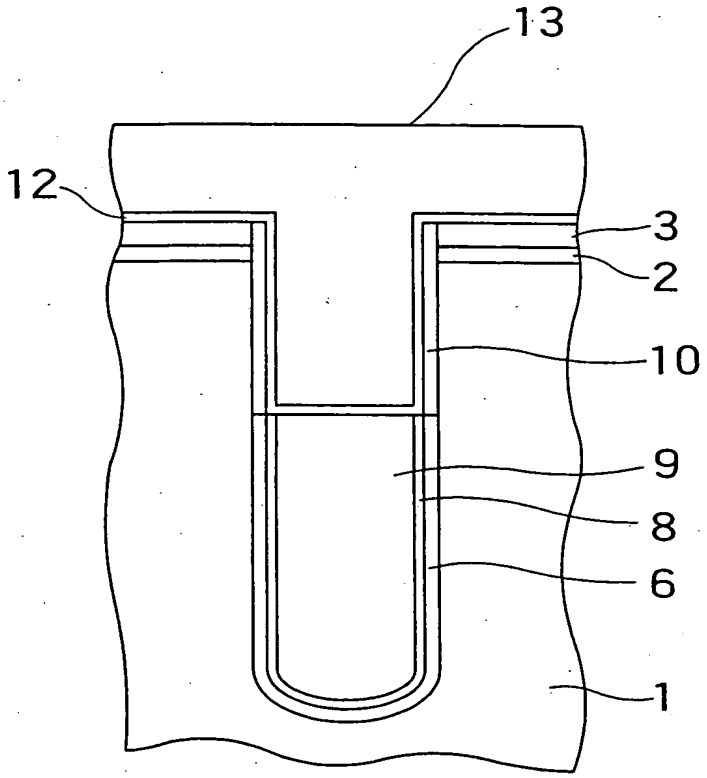


FIG. 8A

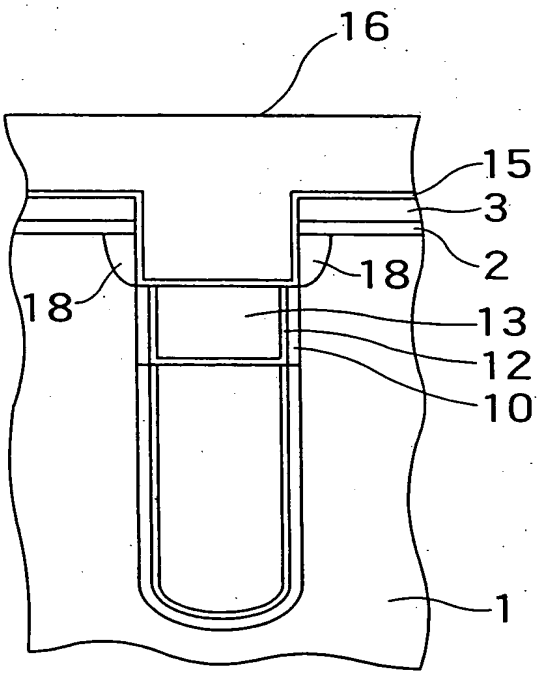


FIG. 8B

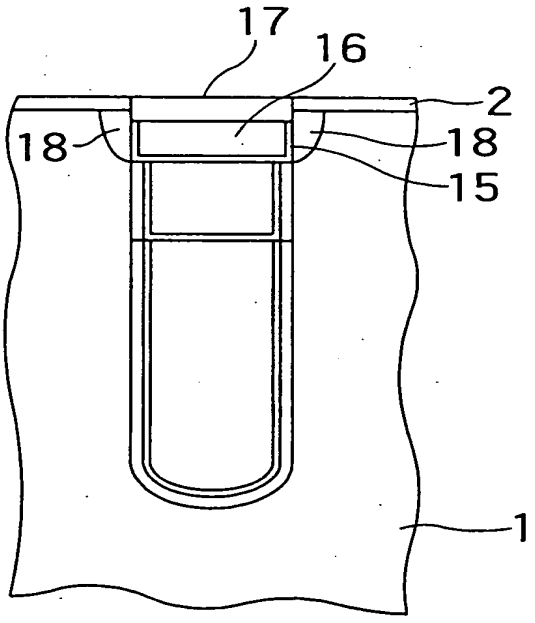


FIG. 8C

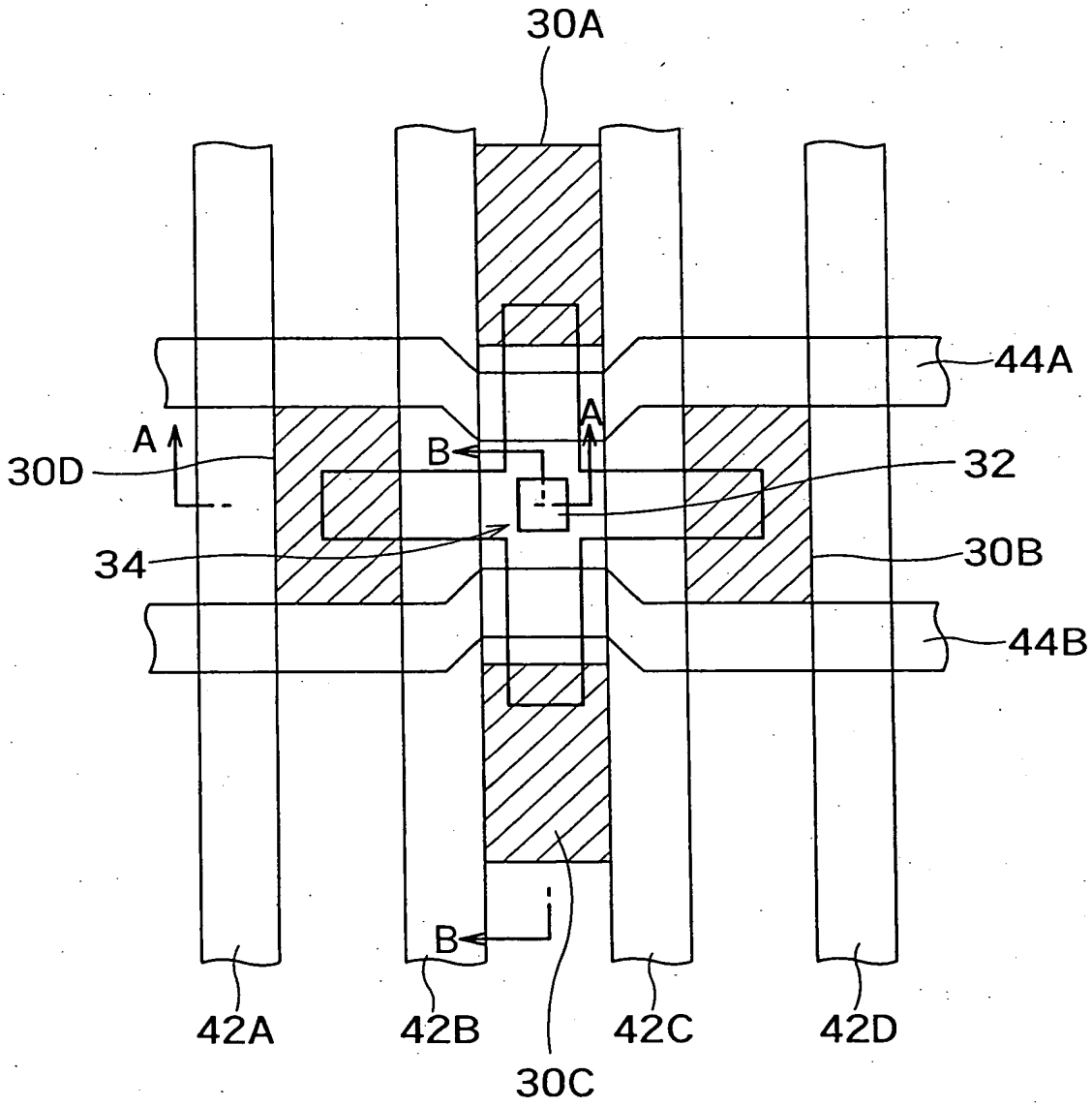


FIG. 9

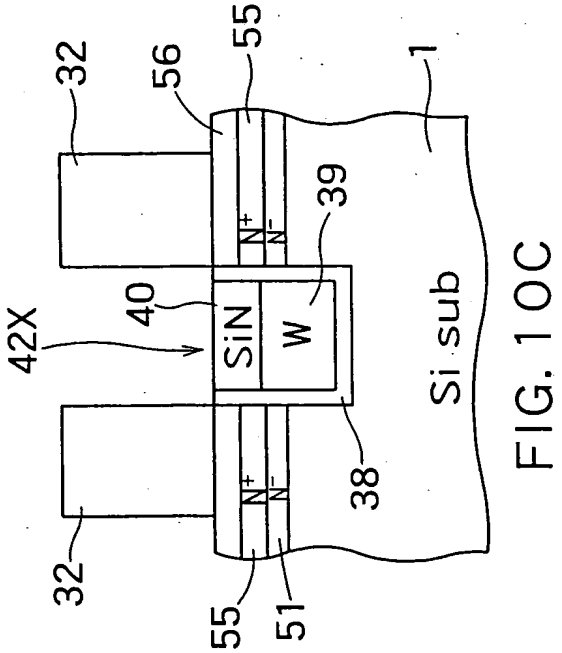


FIG. 10C

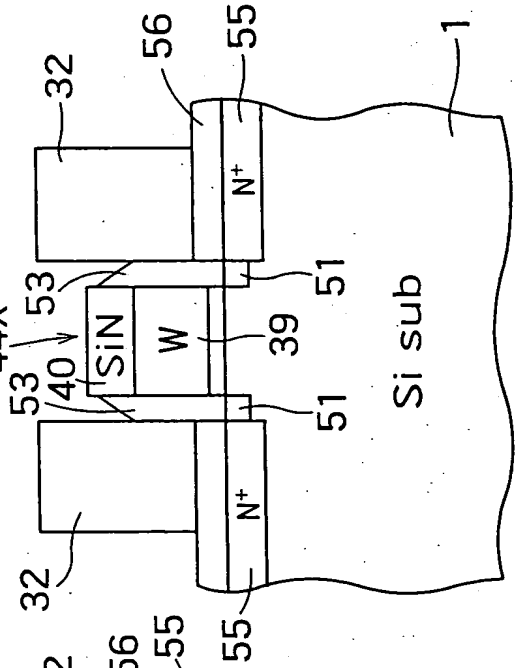


FIG. 10D

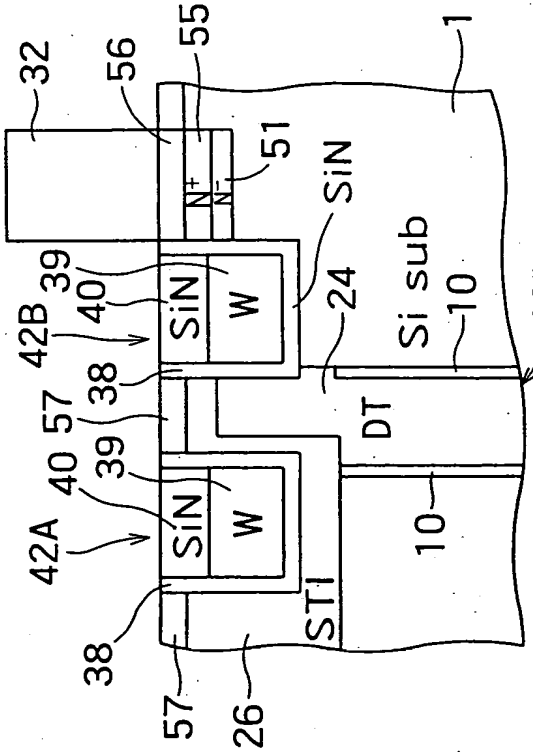


FIG. 10A

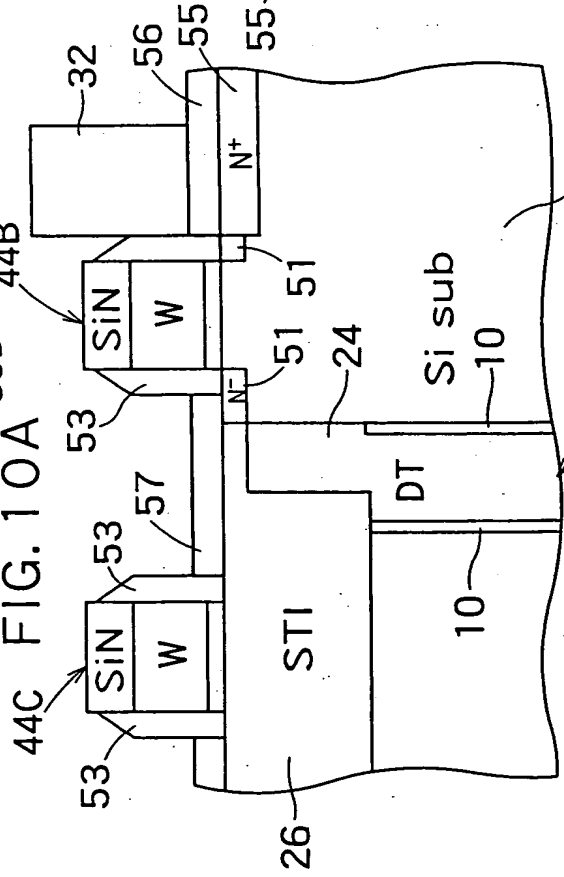


FIG. 10B

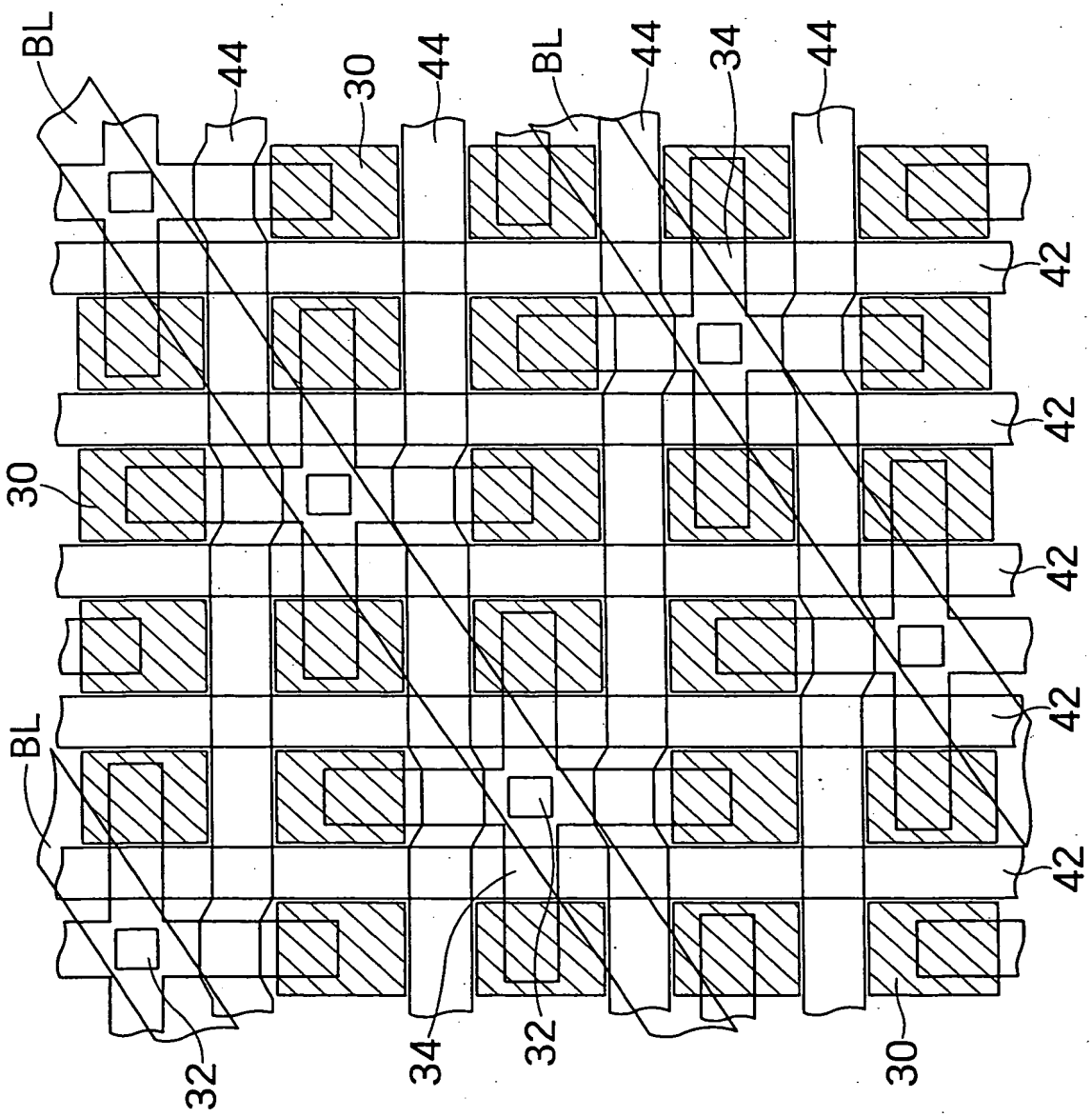
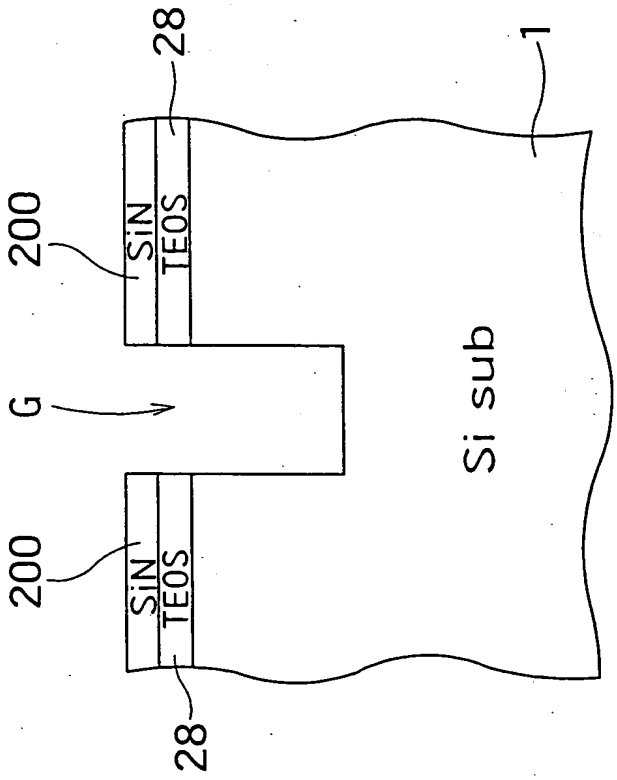
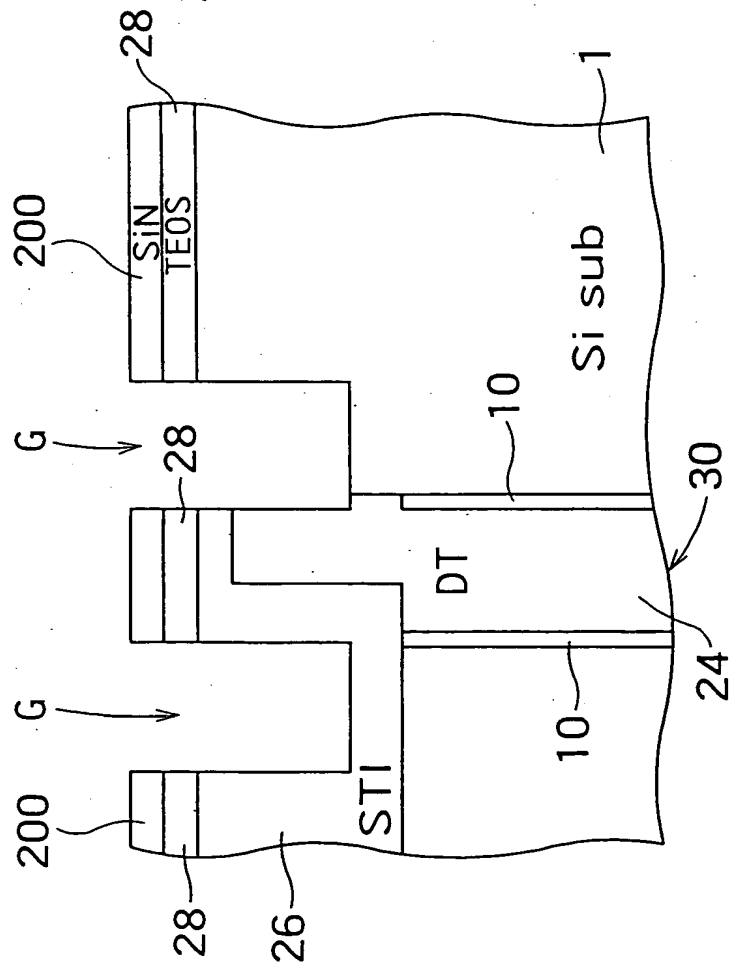


FIG. 11



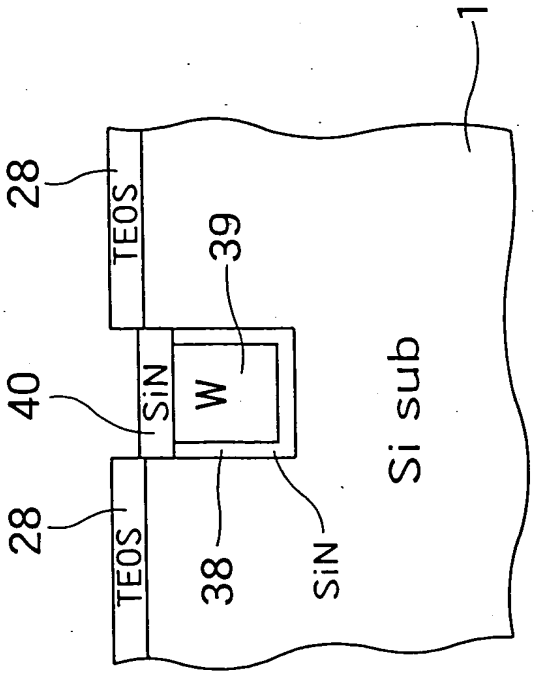
Logic Region

FIG. 12B



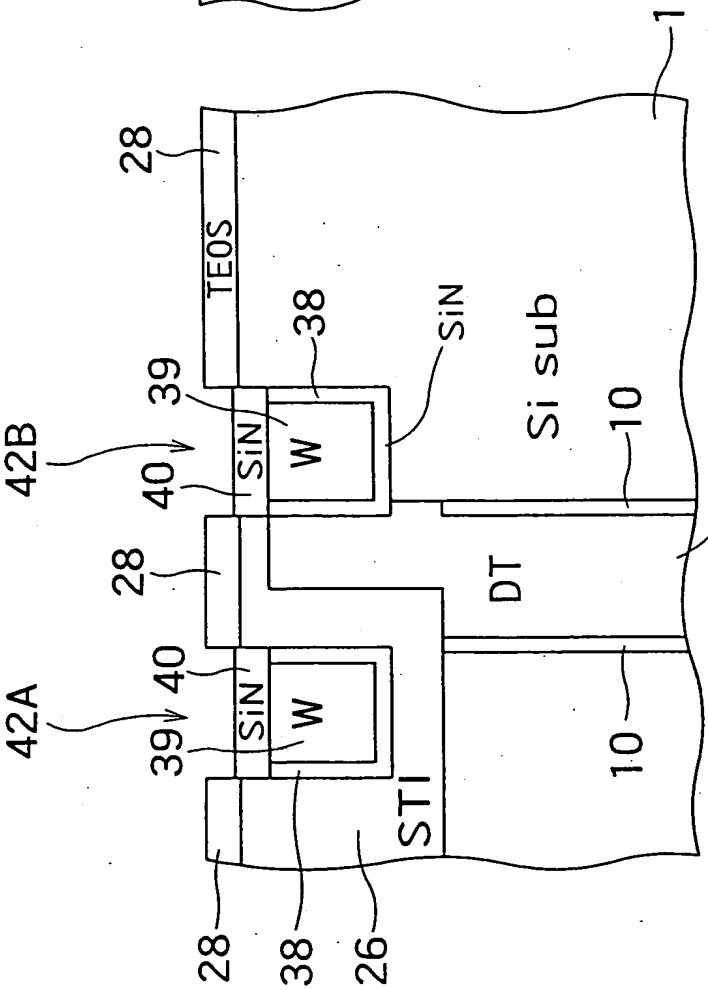
DRAM Array Region

FIG. 12A



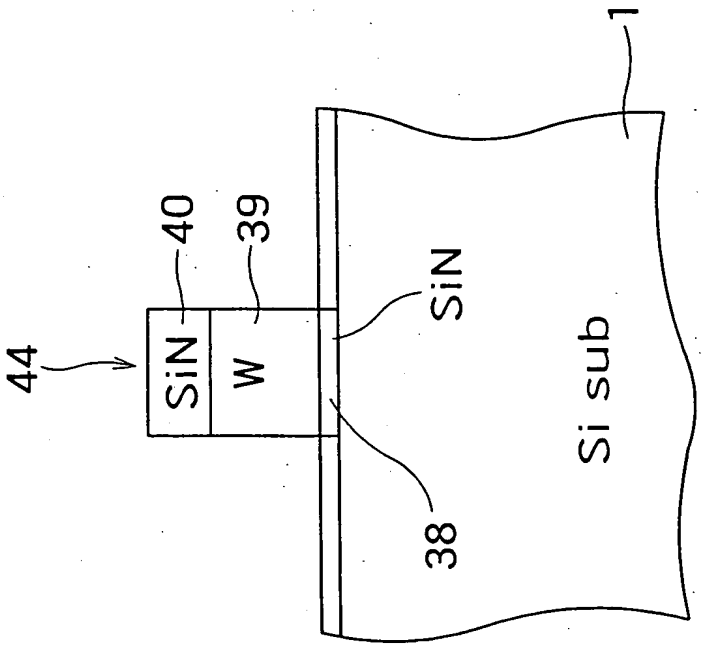
Logic Region

FIG. 13B



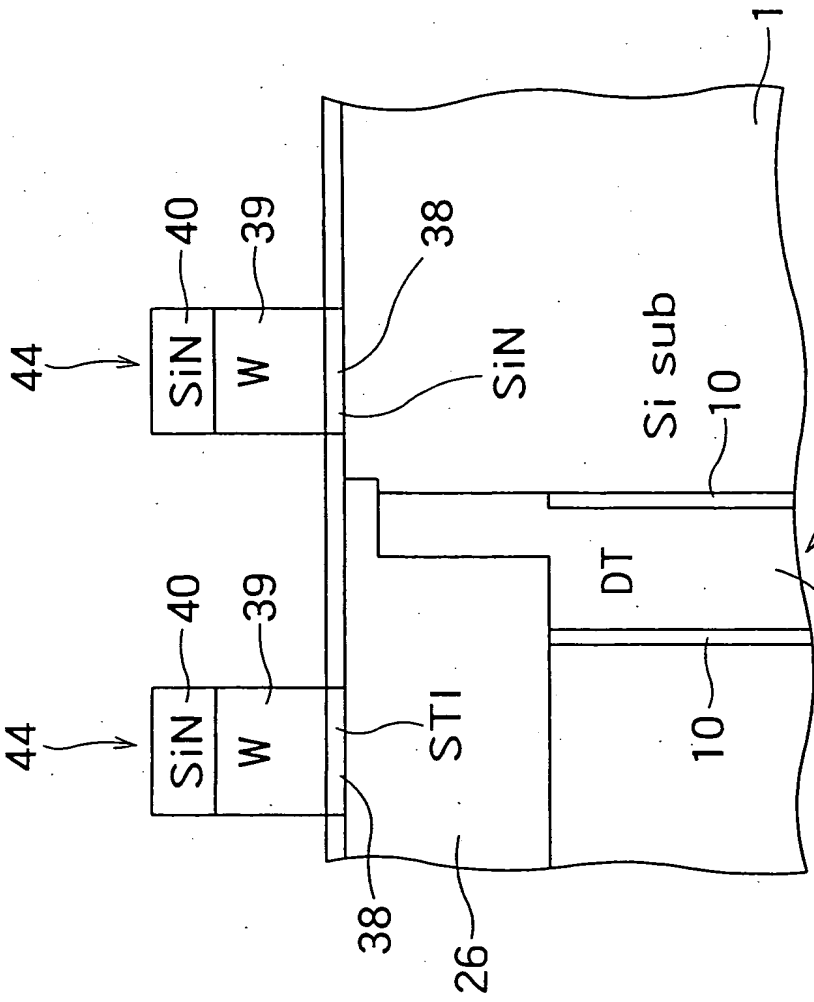
DRAM Array Region

FIG. 13A



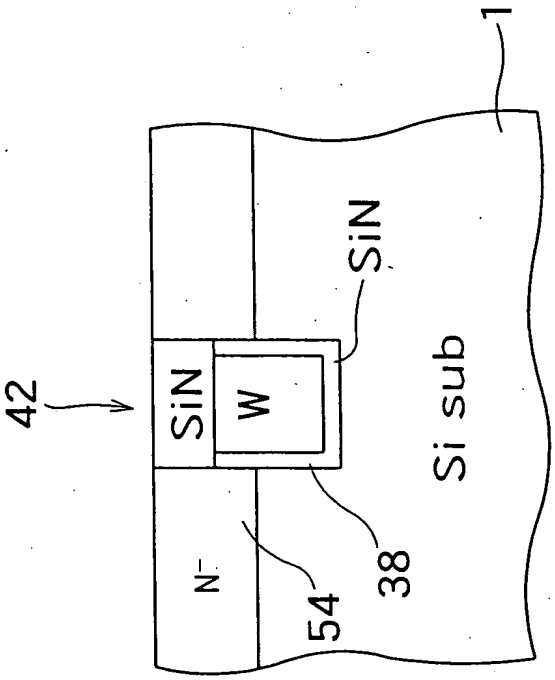
Logic Region

FIG. 14B



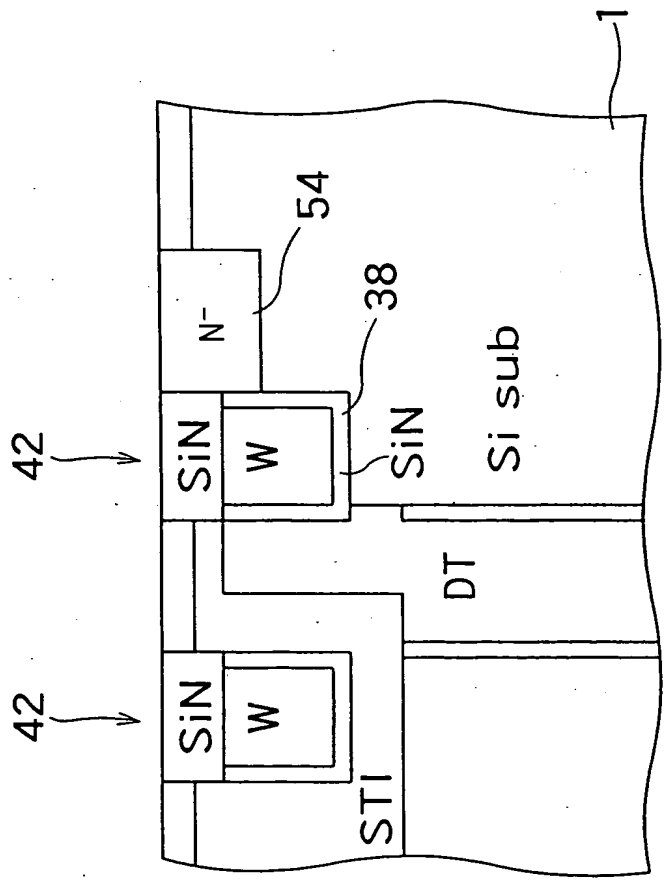
DRAM Array Region

FIG. 14A



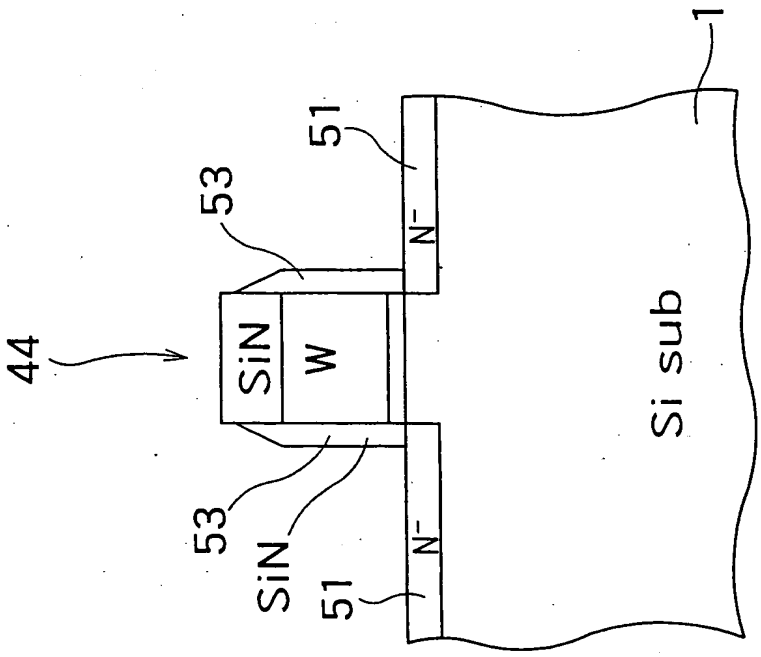
Logic Region

FIG. 15B



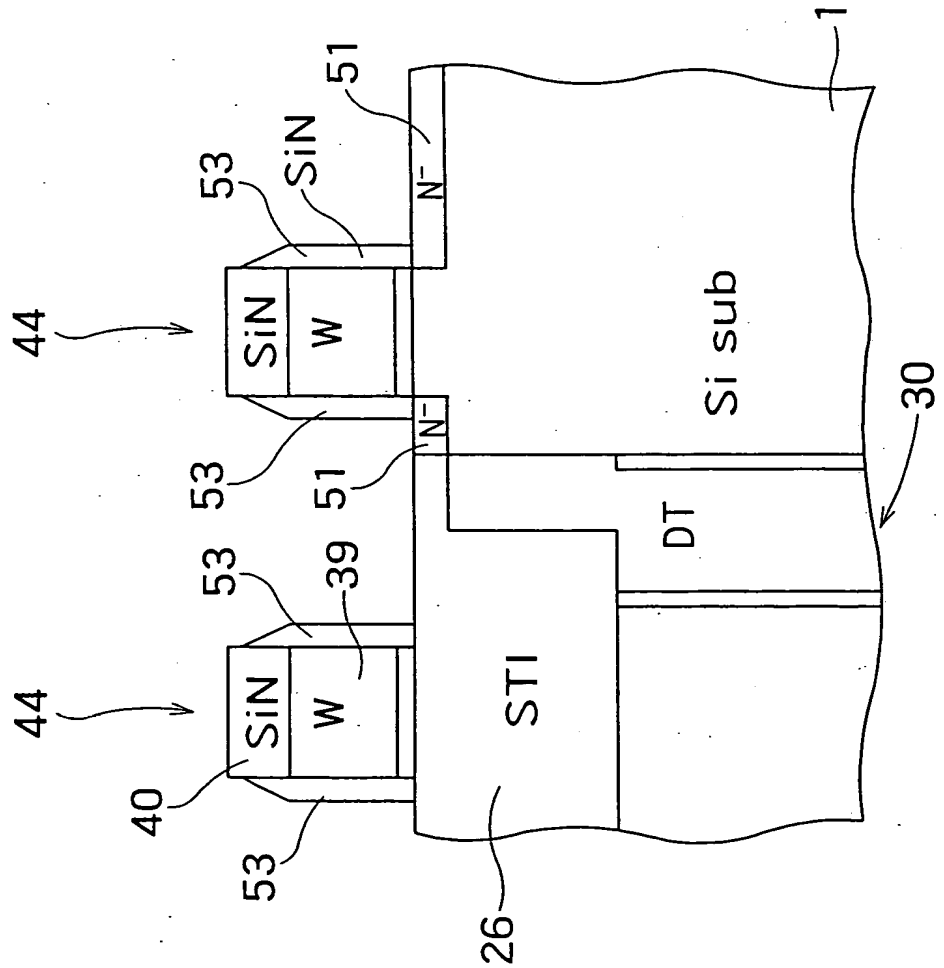
DRAM Array Region

FIG. 15A



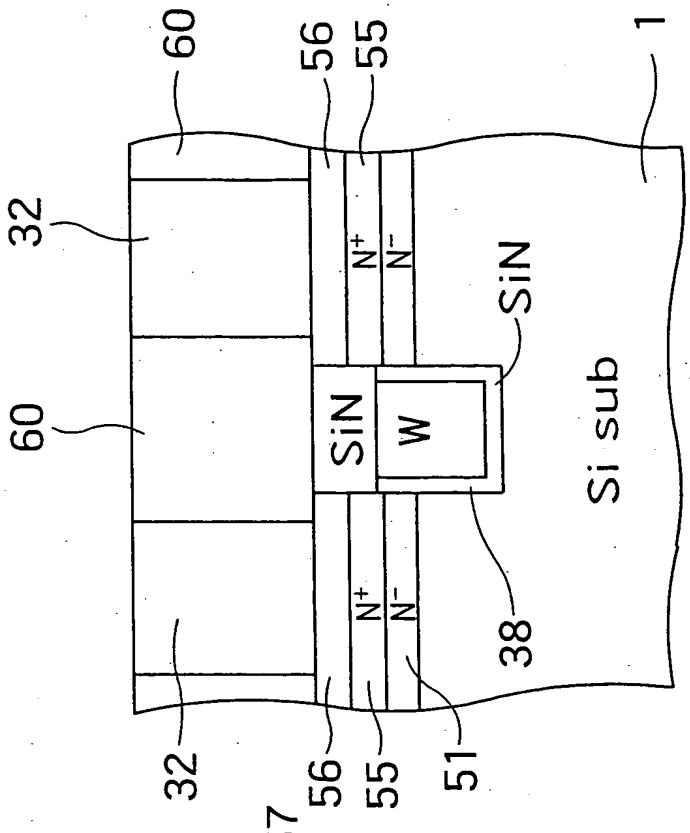
Logic Region

FIG. 16B



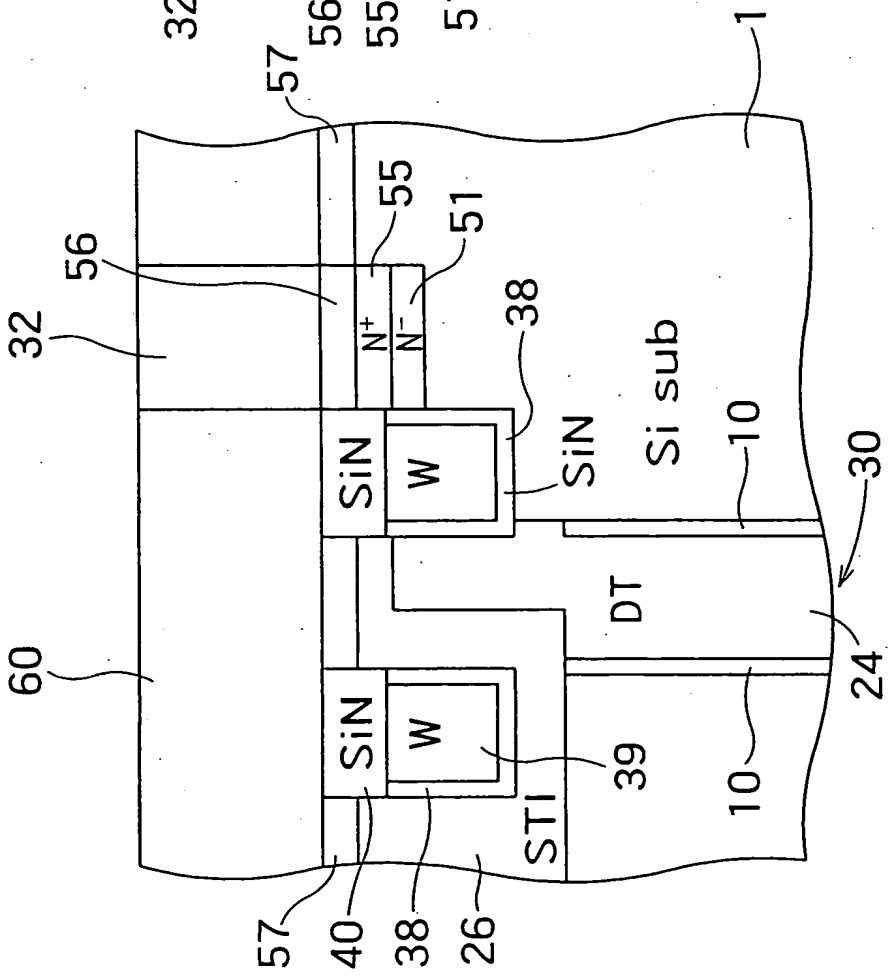
DRAM Array Region

FIG. 16A



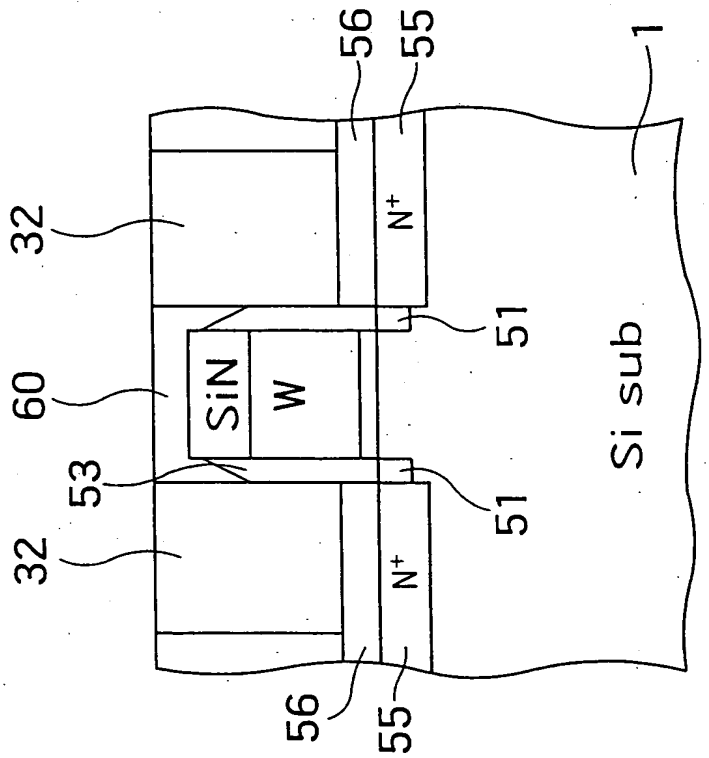
Logic Region

FIG. 17B



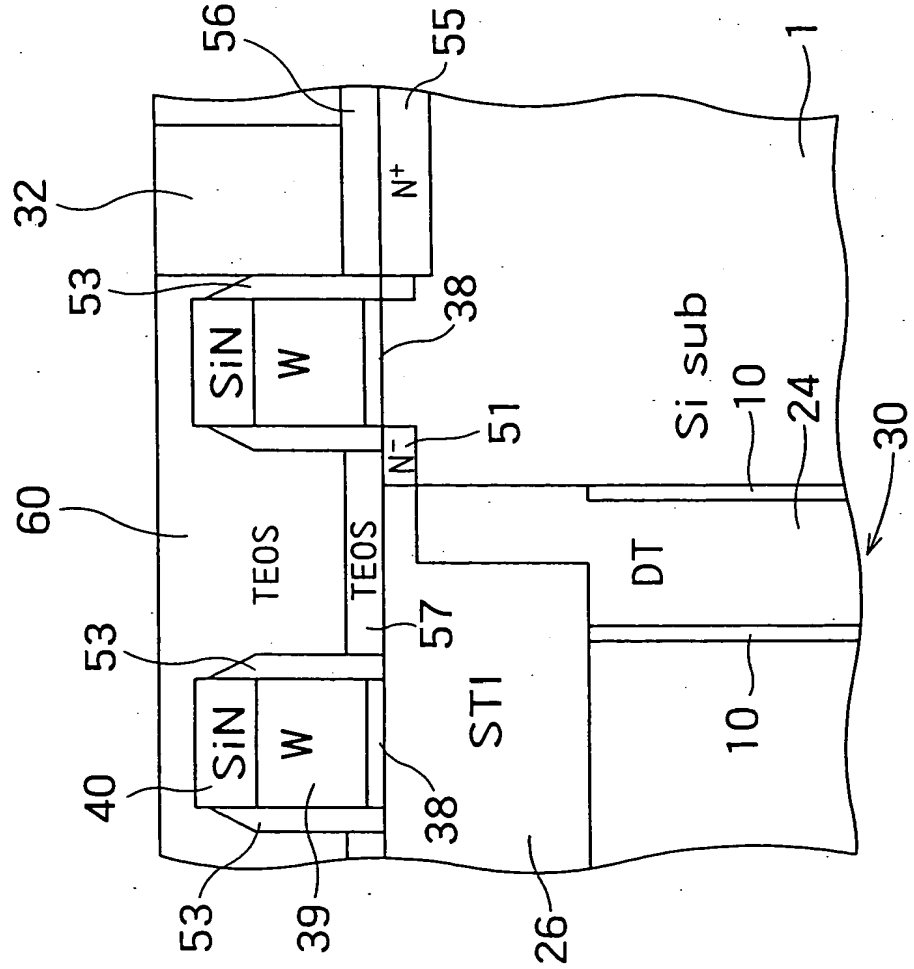
DRAM Array Region

FIG. 17A



Logic Region

FIG. 18B



DRAM Array Region

FIG. 18A

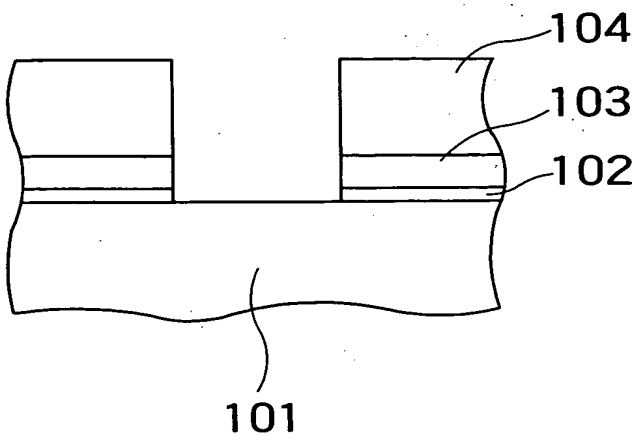


FIG. 19A
(PRIOR ART)

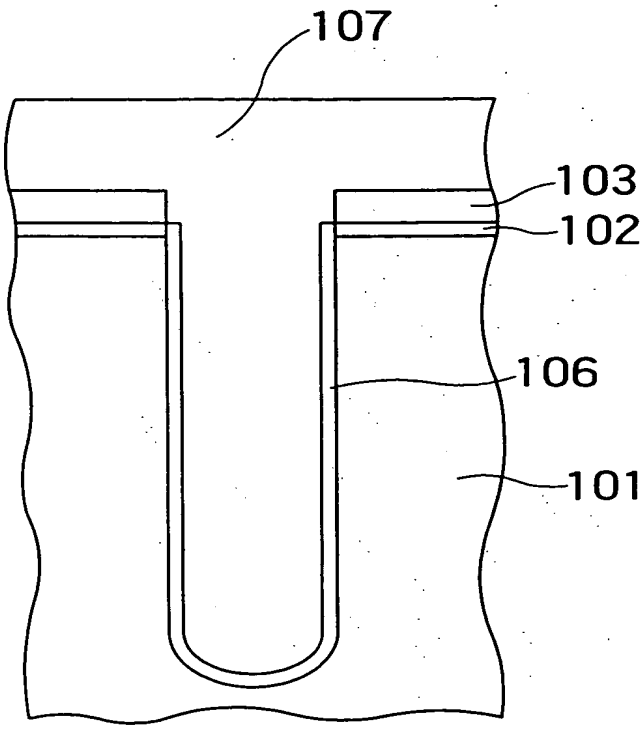


FIG. 19C
(PRIOR ART)

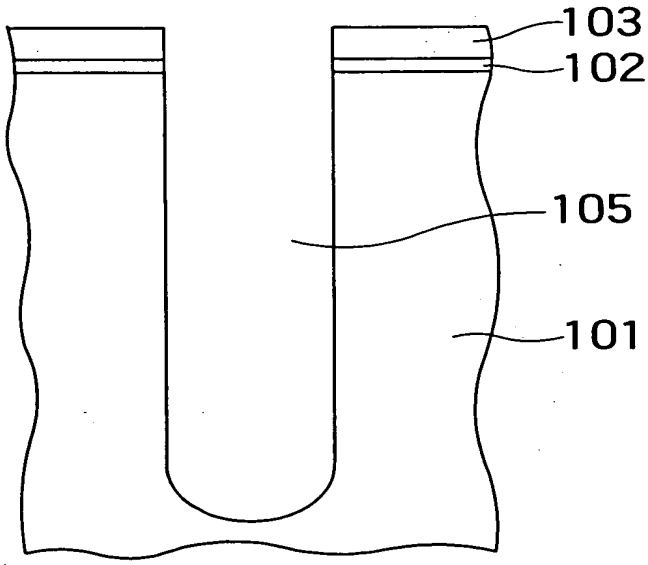


FIG. 19B
(PRIOR ART)

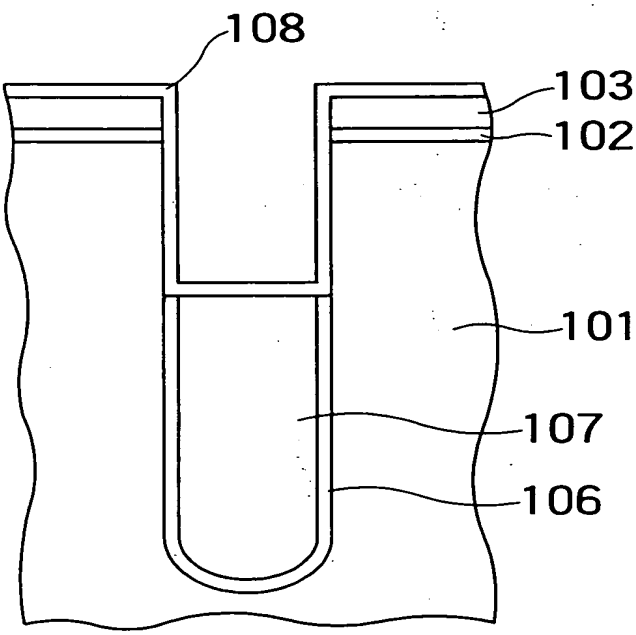


FIG. 19D
(PRIOR ART)

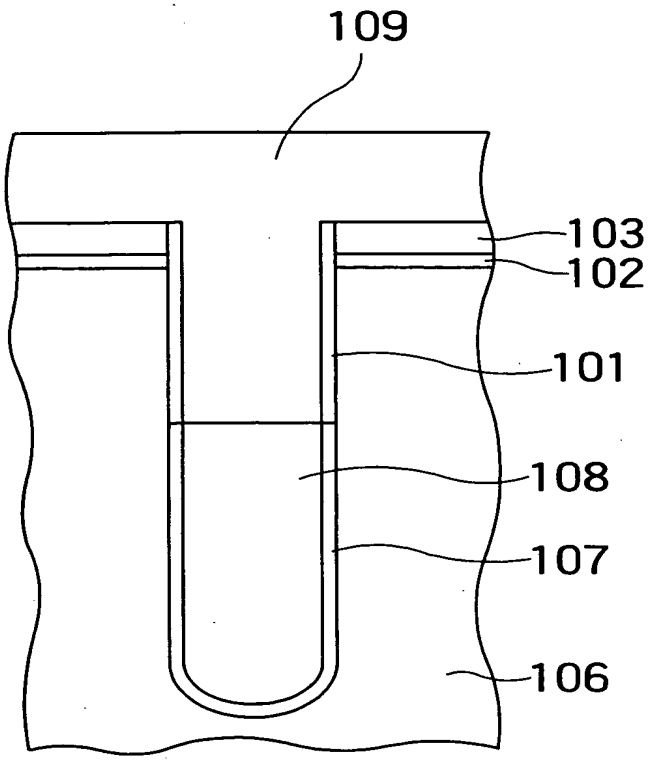


FIG. 20A
(PRIOR ART)

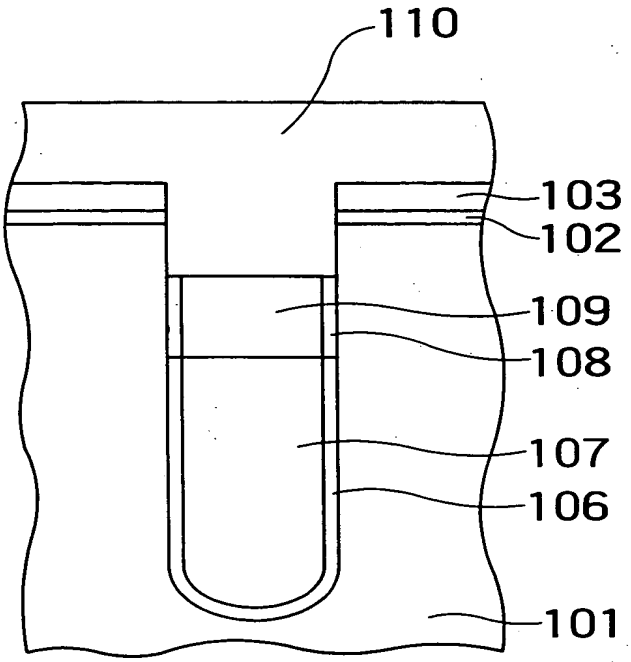


FIG. 20B
(PRIOR ART)

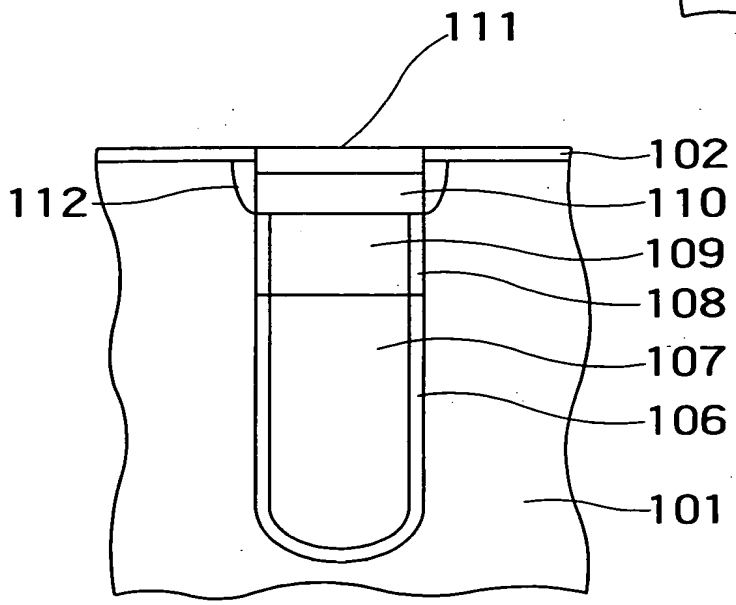


FIG. 20C
(PRIOR ART)